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Coding Style

Every Verilog file should have comments at the beginning. See screen capture Figure 1.

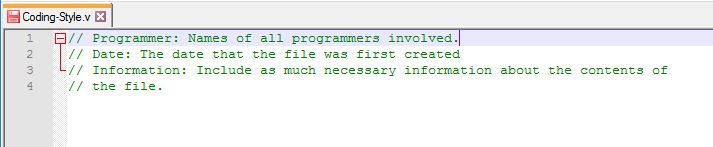


Figure 1.

The code **module** will not be indented. It should line up with the comments. See Figure 2.

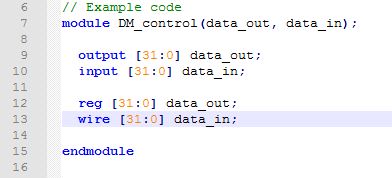


Figure 2.

After the **module**, any immediate variable declarations are indented by 2 spaces. These are immediate declarations. For example, they are located outside of **always** blocks of code. Always indent only with two spaces. See Figure 3.

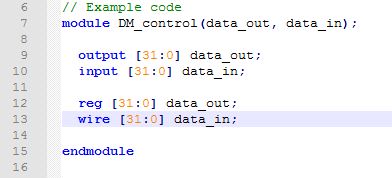


Figure 3.

With regards to variable declarations like **output [ : ]** only include one space in-between each term. Don’t add additional spaces. See Figure 4.

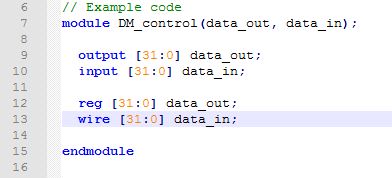


Figure 4.

With regards to the keywords **begin** and **end**, place the **begin** keyword on the starting line of the block of code. The **end** keyword should be place on a separate line of code after the block of code. The indentation of the **end** should be the same as the first line of code where the **begin** keyword is used. See Figure 5.

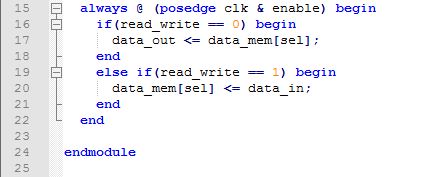


Figure 5.

When a function is called using a lot of arguments, you should place the individual arguments on separate lines. See Figure 6.

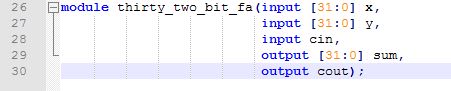
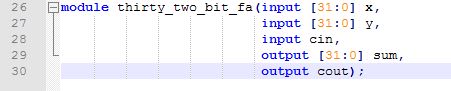


Figure 6.

When naming function or variables, use underscores in-between the unique words. See Figure 7.



The **endmodule** should not have an indentation.